Remarks

In view of the following discussion, the applicants submit that the claims now pending in the application are not obvious under the provisions of 35 U. S. C. § 103. Thus, the applicants believe that all of these claims are in allowable form.

REJECTIONS

A. 35 U. S. C. § 103

1. Claims 1, 5-9, 11/1 and 11/5-11/9 are not unpatentable over Maegawa et al. in view Seki

Claims 1, 5-9, 11/1 and 11/5-11/9 stand rejected under 35 U. S. C. § 103(a) as being unpatentable over Maegawa et al. (U. S. Patent 6,345,018 issued February 2, 2002) in view of Seki (U. S. Patent 3,840,817 issued October 8, 1974). The applicants submit that these claims are not rendered obvious by the combination of these references.

Claim 1 is directed to a method for detecting a wobble signal of an optical disk (*see*, specification at page 1, lines 6-9). In the method, a reference signal corresponding in phase and frequency to an unmodulated wobble signal is generated (by the PLL circuit 212) and then an input signal (IS) including the wobble signal (WS) is compared with a reference signal (RS), the reference signal (RS) corresponding in phase and frequency to the unmodulated wobble signal (*see*, FIG. 2 and the specification at page 2, lines 23-27) and then output as an output signal (OS) indicating the amplitude and the phase of the wobble signal (*see*, FIG. 2 and the specification at page 2, lines 27-29). The comparing step includes generating a sum signal (S1) and a difference signal (S2) of the input signal (IS) and the reference signal (RS) and comparing the amplitudes of

the rectified sum signal (S1) and the rectified difference signal (S2) to obtain the relative phase between the wobble signal (WS) and the reference signal (RS) (*see*, FIG. 2 and the specification at page 2, line 33 to page 3, line 5).

Maegawa et al. uses in an exemplary embodiment the output of a multiplier 20 (*see*, Maegawa et al. at Figs. 2 and 9), to determine the phase error, while in the present application only addition and subtraction operations are needed. This is advantageous in that adders and subtractors can be realized efficiently in digital circuits.

Maegawa et al. further shows an exemplary embodiment which omits the use of a multiplier (*see*, Maegawa et al. at Fig. 6) making use of the same advantage. In this embodiment, the wobble signal and the phase comparison signal are supplied to a subtraction unit 26. Either the output of this circuit or its inverted signal is selected by a selector 29 depending on the phase comparison signal (*see*, Maegawa et al. at column 9, lines 9-30). Computing a sum signal and a difference signal of the wobble signal and the phase comparison signal is not shown by Maegawa et al.

Seki discloses in Fig. 3 an exemplary embodiment which results in a phase sensitive rectification (M, N, D1, D2, Q1, Q2) of two input signals A and B. The phase sensitive rectified signal of the input signals A and B is provided at the output Vout. As intermediate steps to obtain a phase sensitive rectified signal Vout, the sum signal (A+B) and the difference signal (A-B) are calculated and are subsequently squared by the squaring circuits D1 and D2.

The Examiner has indicated in item 2 that performing a phase sensitive rectification of the sum signal and the difference signal is performed by the squaring circuits D1 and D2. This statement is respectfully traversed. The squaring operation of the sum signal and of the difference signal solely does not lead to the same result as performing a phase sensitive rectification of the sum signal and of the difference signal. A squaring operation is related to an absolute value operation, having only positive values as a result. A phase sensitive rectification in contrast may have positive or negative results. Consequently, Seki

does not disclose a phase sensitive rectification of the sum signal (A+B) and the difference signal (A-B) but solely discloses a phase sensitive rectification of the input signals A and B.

Combining the technical teaching proposed by Seki using the embodiment disclosed in Fig. 3 with the technical teaching disclosed by Maegawa et al. would lead to a phase sensitive rectification of the wobble signal and of the phase comparison signal. The phase comparison signal is retrieved directly from the wobble signal. The combination would not lead to the same result as performing a phase sensitive rectification of the sum signal and the difference signal of the wobble signal and of the reference signal and comparing the amplitudes of the rectified sum signal and the rectified difference signal to obtain the relative phase between the wobble signal and the reference signal, as it is disclosed in claim 1. Thus, claim 1 is patentable over Maegawa et al. in view of Seki.

Claims 5-9, 11/1 and 11/5-11/9 depend directly, or indirectly, from claim 1. For the same reasons as stated above for claim 1, claims 5-9, 11/1 and 11/5-11/9 are also patentable over Maegawa et al. in view of Seki.

CONCLUSION

Thus, the applicants submit that none of the claims presently in the application are rendered obvious under the provisions of 35 U. S. C. § 103. Furthermore, the applicants believe that all of the claims satisfy the requirements of 35 U. S. C. § 112.Consequently, the applicants believe that all of the claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending in the application,

it is requested that the Examiner telephone Ms. Patricia A. Verlangieri, at (609) 734-6867. so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

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